

DYNAMIC RANDOM ACCESS MEMORY CELL AND FABRICATING METHOD THEREOF

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1] This application claims the priority benefit of Taiwan application serial no. 931223996, filed August 11, 2004.

BACKGROUND OF THE INVENTION

[Para 2] Field of the Invention

[Para 3] The present invention relates to a memory device and fabricating method thereof. More particularly, the present invention relates to a dynamic random access memory cell and fabricating method thereof.

[Para 4] Description of the Related Art

[Para 5] With each new generation of microprocessor functionally more powerful, the type of software programs that can be operated on is getting bigger and bigger. As a result, memory with an ever-increasing storage capacity and a faster access speed is demanded. Due to the increasing importance of memory storage capacity and operation speed, innovative technique for fabricating memory devices is always a major research target in the semiconductor industry.

[Para 6] In general, memory types can be categorized according to the storage state into volatile memory and non-volatile memory. Dynamic random access memory (DRAM) is a type of volatile memory constructed from an array of memory cells. Each memory cell comprises an active device and a capacitor.

Furthermore, each memory cell is electrically connected to a word line (WL) and a bit line (BL).

[Para 7] According to the type of capacitor used in each memory cell, dynamic random access memory can be further sub-divided into a stack capacitor DRAM and a deep trench capacitor DRAM. Because the deep trench capacitor of a deep trench capacitor DRAM is formed deep within the substrate, planarization is less of a problem compared with a stack capacitor DRAM. Hence, deep trench capacitor DRAM is particularly suitable for fabricating smaller memory devices. However, more and more problems are still encountered in the process of fabricating the deep trench capacitor DRAM as the size of each device is reduced.

[Para 8] Figs. 1A through 1D are schematic cross-sectional views showing the steps for fabricating a portion of a conventional DRAM with a deep trench capacitor. As shown in Fig. 1A, a substrate 100 is provided, and then a patterned pad layer 102 and a mask layer 104 are sequentially formed over the substrate 100. Thereafter, using the patterned pad layer 102 and the mask layer 104 as an etching mask, a deep trench 106 is formed in the substrate 100. A lower electrode 108 is formed in the substrate 100 at the bottom portion of the deep trench 106. After that, a capacitor dielectric layer 110 and a polysilicon layer 112 are sequentially formed over the bottom portion of the deep trench 106. A collar oxide layer 114 is formed over the mask layer 104 and on the exposed interior surface of the deep trench 106 where does the polysilicon layer 112 not cover.

[Para 9] As shown in Fig. 1B, an anisotropic etching process is carried out to remove the collar oxide layer 114 at the top portion of the mask layer 104 and the polysilicon layer 112. The remaining collar oxide layer forms a collar oxide layer 114a on the sidewall of the deep trench 106. Thereafter, polysilicon is deposited into the deep trench 106 to form a polysilicon layer 116.

[Para 10] As shown in Fig. 1C, a portion of the polysilicon layer 116 outside the deep trench 106 and a portion of the polysilicon layer 116 inside the trench 106 are removed to form a polysilicon layer 116a. Thereafter, the

exposed collar oxide layer 114a is removed to form a collar oxide layer 114b. Polysilicon is deposited into the deep trench 106 to form a polysilicon layer 118. The polysilicon layers 112, 116a and 118 are electrically connected together to form the upper electrode of the deep trench capacitor.

[Para 11] As shown in Fig. 1D, a thermal process is carried out to trigger the out-diffusion of dopants inside the polysilicon layer 118 into the substrate 100. Hence, a buried strap (BS) 120 is formed in the substrate 100 around the polysilicon layer 118. The buried strap 120 has a buried strap window 122. Thereafter, a shallow trench isolation (STI) process is carried out to form a STI structure 124 in the substrate 100 adjacent to the polysilicon layer 118 and form a polysilicon layer 118a. The STI structure 124 also defines an active region (not shown). After that, the pad layer 102 and the mask layer 104 are removed. Then, a gate structure 126 is formed on the active region of the substrate 100 and another gate structure 128 is formed on the STI structure 124. A source region 130a and a drain region 130b are formed in the substrate 100 on each side of the gate structure 126. The drain region 130b is electrically connected to the upper electrode of the deep trench capacitor through the buried strap 120.

[Para 12] However, the size of the buried strap window 122 formed by the aforementioned DRAM fabrication process influences the performance of the DRAM device. For example, if the buried strap window is too large, leakage current will be a significant problem for the device. On the other hand, if the buried strap window is too small, the resistance between the buried strap and the upper electrode may be too high leading to a significant drop in the performance of the device. Therefore, the size of the buried strap window has become one of the critical factors affecting the performance of DRAM devices.

SUMMARY OF THE INVENTION

[Para 13] Accordingly, at least one objective of the present invention is to provide a method of fabricating a dynamic random access memory cell capable of resolving the problem resulting from too large or too small a buried strap window.

[Para 14] At least a second objective of the present invention is to provide an alternative method of fabricating a dynamic random access memory cell capable of resolving the problem resulting from too large or too small a buried strap window.

[Para 15] At least a third objective of the present invention is to provide a dynamic random access memory cell capable of resolving the problem resulting from too large or too small a buried strap window.

[Para 16] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of fabricating a dynamic random access memory (DRAM) cell. First, a substrate having a patterned mask layer thereon and a deep trench therein is provided. The patterned mask layer exposes the deep trench. A lower electrode is formed in the substrate at a bottom portion of the deep trench and a capacitor dielectric layer is formed on the exposed surface of the deep trench. Thereafter, a conductive material is deposited into the bottom portion of the deep trench to form a first conductive layer. The capacitor dielectric layer not covered by the first conductive layer is removed. After that, a collar oxide layer is formed on the sidewall of the deep trench exposed by the first conductive layer. A second conductive material is deposited into the deep trench to form a second conductive layer over the first conductive layer. A trench is formed in the substrate on one side of the second conductive layer. The trench exposes a portion of the substrate and the second conductive layer. Thereafter, a semiconductor strip is formed inside the trench such that the semiconductor strip exposes a portion of the substrate at the bottom portion of the trench. One end of the semiconductor strip is adjacent to the second conductive layer while the other end of the semiconductor strip is adjacent to the substrate. A gate dielectric layer is formed over the substrate to cover the exposed semiconductor strip and the

substrate. Then, a gate is formed over the gate dielectric layer such that the gate crosses over the semiconductor strip and the portion of the semiconductor strip underneath the gate serves as a channel region.

[Para 17] The present invention also provides an alternative method of fabricating a dynamic random access memory (DRAM) cell. First, a substrate having a patterned mask layer thereon and a deep trench capacitor therein is provided. The deep trench capacitor comprises a lower electrode, an upper electrode, a capacitor dielectric layer and a collar oxide layer. The patterned mask layer exposes the upper electrode of the deep trench capacitor. Thereafter, a trench is formed in the substrate on one side of the deep trench capacitor. The trench exposes a portion of the substrate and the upper electrode. A semiconductor material is deposited into the trench to form a semiconductor material layer. After that, the semiconductor material layer is patterned to form a semiconductor strip and a pair of openings that expose a portion of the substrate. One end of the semiconductor strip is adjacent to the upper electrode while the other end of the semiconductor strip is adjacent to the substrate. A gate dielectric layer is formed over the substrate to cover the exposed semiconductor strip and substrate. Next, a conductive layer is formed over the gate dielectric layer. The conductive layer crosses over the semiconductor strip and the portion of the semiconductor strip underneath the conductive layer serves as a channel region.

[Para 18] The present invention also provides a dynamic random access memory (DRAM) cell. The DRAM cell comprises a deep trench capacitor and an active device. The deep trench capacitor is disposed inside the deep trench in the substrate. The deep trench capacitor comprises a lower electrode, an upper electrode, a capacitor dielectric layer and a collar oxide layer. The lower electrode is disposed in the substrate at the bottom portion of the deep trench. The upper electrode is disposed in the deep trench. The capacitor dielectric layer is disposed between the bottom surface of the deep trench and the upper electrode. The collar oxide layer is disposed on the sidewall of the deep trench not covered by the capacitor dielectric layer, and is between the upper electrode and the substrate. The active device is disposed in a trench in

the substrate adjacent to the deep trench capacitor. Furthermore, the active device comprises a semiconductor strip, a gate dielectric layer, a gate and a doped region. The semiconductor strip is disposed in the trench and exposes a portion of the substrate at the bottom portion of the trench. One end of the semiconductor strip is adjacent to the substrate while the other end of the semiconductor strip is adjacent to the upper electrode. In addition, the gate dielectric layer is disposed on the surface of the semiconductor strip. The gate is disposed on the gate dielectric layer. The gate crosses over the semiconductor strip, and the gate-covered portion of the semiconductor strip serves as a channel region. The doped region is disposed in a portion of the semiconductor strip adjacent to the substrate and the adjacent substrate thereof.

[Para 19] In the present invention, the portion of the semiconductor strip covered by the gate of an active device serves as a channel region. Furthermore, the semiconductor strip is adjacent to the conductive layer (or the top portion of the upper electrode) of the deep trench capacitor. Hence, there is no need to form a buried strap for electrically connecting with the active device. Therefore, the present invention is capable of resolving the problem resulting from too large or too small a buried strap window.

[Para 20] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 21] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[Para 22] Figs. 1A through 1D are schematic cross-sectional views showing the steps for fabricating a portion of a conventional DRAM with a deep trench capacitor.

[Para 23] Fig. 2 is a top view of a dynamic random access memory cell according to one preferred embodiment of the present invention.

[Para 24] Fig. 3 is a schematic cross-sectional view along line I-I' of the dynamic random access memory cell shown in Fig. 2.

[Para 25] Fig. 4 is a perspective view of a portion of the dynamic random access memory cell shown in Fig. 2.

[Para 26] Figs. 5A through 5E are schematic cross-sectional views along line I-I' in Fig. 2 for showing the steps of fabricating a dynamic random access memory cell.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Para 27] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[Para 28] Fig. 2 is a top view of a dynamic random access memory cell according to one preferred embodiment of the present invention. Fig. 3 is a schematic cross-sectional view along line I-I' of the dynamic random access memory cell shown in Fig. 2. As shown in Figs. 2 and 3, the dynamic random access memory cell of the present invention comprises a deep trench capacitor 201 and an active device 203. The deep trench capacitor 201 is disposed inside a deep trench 206 within a substrate 200. The deep trench capacitor 201 comprises a lower electrode 208, an upper electrode 205, a capacitor dielectric layer 210a and a collar oxide layer 214. In one preferred embodiment, the upper electrode 205 comprises conductive layers 212 and 216. The active device 203 is disposed in another trench 218 in the substrate 200 adjacent to the deep trench capacitor 201. The active device 203 comprises a semiconductor strip 228b, a gate dielectric layer 230, a

conductive layer 232a and a doped region 236. In one preferred embodiment, extension portions 228a and 228c are attached to each end of the semiconductor strip 228b to form an H-shaped semiconductor layer 224.

[Para 29] The lower electrode 208 of the deep trench capacitor 201 is disposed in the substrate 200 at the bottom portion of the deep trench 206. The conductive layer 212 is disposed at the bottom portion of the deep trench 206. Furthermore, the capacitor dielectric layer 210a is disposed between the surface of the bottom portion of the deep trench 206 and the conductive layer 212. The conductive layer 216 is disposed over the conductive layer 212 and completely fills the deep trench 206. The collar oxide layer 214 is disposed between the conductive layer 216 and the substrate 200.

[Para 30] The semiconductor strip 228b of the active device 203 is disposed inside the trench 218. The semiconductor strip 228b exposes a portion of the substrate 200 at the bottom portion of the trench 218. The extension portion 228a is positioned next to the conductive layer 216 while the extension portion 228c is positioned next to the substrate 200. Obviously, the semiconductor strip 228b can be only disposed inside the trench 218 in another embodiment so that the ends of the semiconductor strip 228b are positioned next to the conductive layer 216 and the substrate 200, respectively. The semiconductor strip 228b and the extension portions 228a and 228c are fabricated from, for example, epitaxial silicon or other suitable semiconductor material for forming a channel. In one preferred embodiment, a portion of the substrate 200 outside the trench 218 may also be exposed (e.g. an enclosed area 226 by dash line in Fig. 2) aside from that portion of the substrate at the bottom of the trench 218.

[Para 31] The gate dielectric layer 230 is disposed on the semiconductor strip 228b and the extension portions 228a and 228c. In one preferred embodiment, the gate dielectric layer 230 may also be disposed on the top surface of the conductive layer 216.

[Para 32] The conductive layer 232a is disposed on a portion of the gate dielectric layer 230. The conductive layer 232a crosses over the semiconductor strip 228b, and the portion of the semiconductor strip 228b

covered by the conductive layer 232a serves as a channel region 207. Fig. 4 is a perspective view showing the conductive layer 232a crossing over the semiconductor strip 228b (the labeled area 233 in Fig. 2). Since the conductive layer 232a covers the two sidewalls 234a and the top portion 234b of the semiconductor strip 228b, the active device 203 is able to avoid some problems resulting from short channel effect. In addition, the conductive layer 232a may serve as a gate of a single memory cell or a word line for serially connecting an array of memory cells.

[Para 33] The doped region 236, which serves as a source region, is disposed in a portion of the extension portion 228c of the semiconductor strip 228b and in a portion of the substrate 200 adjacent to the extension portion 228c of the semiconductor strip 228b.

[Para 34] In another embodiment, the dynamic random access memory cell further comprises a doped stripe 220 disposed in the substrate 200 adjacent to the lower electrode 208.

[Para 35] In yet another embodiment, the dynamic random access memory cell further comprises a doped well 222 disposed within a portion of the conductive layer 216 and its adjacent substrate 200. Additionally, the trench 218 is disposed in the doped well 222.

[Para 36] Furthermore, in yet another embodiment, the dynamic random access memory cell further comprises a doped stripe 220 disposed in the substrate 200 and a doped well 222 disposed in a portion of the conductive layer 216 and its adjacent substrate 200. The doped stripe 220 is adjacent to the lower electrode 208 and the doped well 222. In addition, the doped well 222 and the doped stripe 220 are doped with opposite type of dopants.

[Para 37] In the present invention, the portion of the semiconductor strip covered by the conductive layer (the gate) serves as a channel region. Furthermore, the semiconductor strip or its extension portion is adjacent to the conductive layer (or the top portion of the upper electrode) of the deep trench capacitor. Hence, there is no need to form a buried strap for electrically connecting the deep trench capacitor with the active device. Therefore, the

present invention is capable of resolving the problem resulting from too large or too small a buried strap window.

[Para 38] Figs. 5A through 5E are schematic cross-sectional views showing the steps of fabricating a dynamic random access memory cell. As shown in Fig. 5A, a substrate 200 is provided. After forming a pad layer 202 over the substrate 200 blankly, a mask layer 204 is formed over the pad layer 202. The pad layer 202 is a silicon oxide layer formed by, for example, performing a thermal oxidation process. The mask layer 204 is a silicon nitride layer formed by, for example, performing a chemical vapor deposition (CVD) process. Thereafter, photolithographic and etching processes are carried out to pattern the mask layer 204 and the pad layer 202. Using the patterned mask layer 204 and the pad layer 202 as a mask, an etching process is carried out to form a deep trench 206 in the substrate 200. The substrate 200 is etched in a dry etching process, for example.

[Para 39] After that, a lower electrode 208 is formed in the substrate 200 at the bottom portion of the deep trench 206. The lower electrode 208 is a doped region, for example. The lower electrode 208 is formed, for example, by depositing a doped insulating material on the sidewalls of the bottom portion of the deep trench 206 to form a doped insulation layer, and then filling the deep trench 208 with a photoresist material. Thereafter, the doped insulation layer uncovered by the photoresist layer is removed. After removing the photoresist layer, a conformal insulating layer is formed. A thermal process is carried out to trigger dopants of the doped insulation layer diffusing into the substrate 200. Finally, the insulation layer and the doped insulation layer are removed. In one preferred embodiment, the lower electrode 208 is doped with n-type material. Since the fabrication of the lower electrode 208 is a known art, detailed description is omitted herein.

[Para 40] A conformal capacitor dielectric layer 210 is formed over the mask layer 204 and the interior surface of the deep trench 206. The capacitor dielectric layer 210 is, for example, a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer or other suitable dielectric material layer. The

capacitor dielectric layer 210 is formed, for example, by performing thermal oxidation, chemical vapor deposition or some other suitable processes.

[Para 41] Conductive material is deposited into the bottom portion of the deep trench 206 to form a conductive layer 212 covering a portion of the capacitor dielectric layer 210. The conductive layer 212 is fabricated, for example, using polysilicon, doped polysilicon or other suitable conductive material. The conductive layer 212 is formed, for example, by performing a chemical vapor deposition process with in-situ ion implant to form a doped polysilicon layer over the substrate 200, and then removing the doped polysilicon layer outside the deep trench 206 and a portion of the doped polysilicon layer at the top portion of the deep trench 206. The method of removing a portion of the doped polysilicon includes, for example, a dry etching process or a wet etching process. Aside from the in-situ ion implant for forming the doped polysilicon layer, it is possible to form the doped polysilicon layer by introducing a dopant-containing reactive gas into the reaction chamber during the chemical vapor deposition.

[Para 42] As shown in Fig. 5B, the capacitor dielectric layer 210 not covered by the conductive layer 212 is removed to form a capacitor dielectric layer 210a. The method of removing a portion of the capacitor dielectric layer 210 includes performing a dry etching or a wet etching process, for example.

[Para 43] A collar oxide layer 214 is formed on the sidewall of the deep trench 206 exposed by the conductive layer 212. The collar oxide layer 214 is a silicon oxide layer formed by, for example, performing a chemical vapor deposition process to produce a conformal collar oxide material layer over the substrate 200. Thereafter, the collar oxide material layer outside the deep trench 206 and the collar oxide material layer above the conductive layer 212 inside the deep trench 206 are removed. The method of removing a portion of the collar oxide material layer includes, for example, performing an anisotropic etching process.

[Para 44] Thereafter, conductive material is deposited into the deep trench 206 to form a conductive layer 216 and covers the conductive layer 212. The conductive layer 216 is electrically connected to the conductive layer

212. The conductive layers 216 and 212 form the upper electrode 205 of the deep trench capacitor. Since the conductive 216 is fabricated using a material and a process similar to the conductive layer 212, detailed description is omitted.

[Para 45] The processes for fabricating the active device are carried out next. As shown in Fig. 5C, another trench 218 is formed in the substrate 200 on one side of the conductive layer 216. The trench 218 exposes a portion of the substrate 200 and the conductive layer 216. The trench 218 is formed by an etching process, for example. In one preferred embodiment, a doped stripe 220 is formed in the substrate 200 adjacent to the lower electrode 208 before forming the trench 218. The doped stripe 220 is a region of n-doped material, for example. In another preferred embodiment, before forming the trench 218, a doped well 222 is formed in a portion of the conductive layer 216 and its adjacent substrate 200 where is designated for forming the trench 218 so that the trench 218 is formed within the doped well 222. The doped well 222 is a region of p-doped material, for example. In yet another preferred embodiment, before forming the trench 218, a doped stripe 220 is formed in the substrate 200 and a doped well 222 is formed in a portion of the conductive layer 216 and its adjacent substrate 200 where is designated for forming the trench 218. The doped stripe 220 is adjacent to the lower electrode 208 and the doped well 222. Furthermore, the doped stripe 220 and the doped well 222 are doped using opposite type of dopants.

[Para 46] Semiconductor material is deposited into the trench 218 to form a semiconductor material layer 223. The semiconductor material layer 223 is fabricated using epitaxial silicon or other suitable channel material, and the semiconductor material is deposited by a chemical deposition process, for example.

[Para 47] Referring to Fig. 5D and Fig. 2, the semiconductor material layer 223 is patterned to form a semiconductor strip 228b in the trench 218. In one preferred embodiment, a portion of the mask layer 204, the pad layer 202 and the substrate 200 are removed to form two openings (enclosed area 226 by dash line in Fig. 2) that expose the substrate 200. In another preferred

embodiment, the process of forming the semiconductor strip 228b in the trench 218 further includes forming extension portions 228a and 228c on each end of the semiconductor strip 228b to form an H-shaped semiconductor layer 224. The extension portion 228a is adjacent to the conductive layer 216 while the other extension portion 228c is adjacent to the substrate 200. The semiconductor strip 228b and its extension portions 228a and 228c are fabricated using, for example, epitaxial silicon or other semiconductor material suitable for forming a channel.

[Para 48] A gate dielectric layer 230 is formed over the substrate 200 to cover the exposed semiconductor strip 228b, the extension portions 228a and 228c and the substrate 200. The gate dielectric layer 230 is a silicon oxide layer formed by, for example, performing a thermal oxidation process. In one preferred embodiment, the gate dielectric layer 230 is formed on the top surface of the conductive layer 216. Thereafter, a conductive layer 232 is formed over the substrate 200 to cover the gate dielectric layer 230.

[Para 49] As shown in Fig. 5E, a portion of the conductive layer 232 is removed to form a conductive layer 232a over a portion of the gate dielectric layer 230. The conductive layer 232a crosses over the semiconductor strip 228b, and the portion of the semiconductor strip 228b covered by the conductive layer 232a serves as a channel region 207 (as shown in Fig. 2). Fig. 4 is a perspective view showing the conductive layer 232a crossing over the semiconductor strip 228b (the labeled area 233 in Fig. 2). It should be noted that the conductive layer 232a covers the two sidewalls 234a and the top portion 234b of the semiconductor strip 228b that is used as a channel region. Hence, the active device 203 is able to avoid some problems induced by short channel effect. In addition, the conductive layer 232a may serve as a gate of a single memory cell or a word line for serially connecting an array of memory cells.

[Para 50] In one preferred embodiment, a doped region 236 serving as a source region is formed in a portion of the extension portion 228c of the semiconductor strip 228b and the substrate 200 adjacent to the extension portion 228c.

[Para 51] In addition, an interconnect process for electrically connecting the doped region 236 and the conductive layer 232a with an external circuit through a contact is performed after forming the doped region 236.

[Para 52] In the present invention, the portion of the semiconductor strip covered by the conductive layer (the gate) of the active device serves as a channel region. Furthermore, the semiconductor strip is adjacent to the conductive layer (or the top portion of the upper electrode) of the deep trench capacitor. Hence, there is no need to form a buried strap for electrically connecting the deep trench capacitor with the active device. Therefore, the present invention is capable of resolving the problem resulting from too large or too small a buried strap window.

[Para 53] The aforementioned steps for fabricating the deep trench capacitor serve to illustrate the spirit of the present invention only and hence should by no means limit the scope of the present invention. In other words, other process of fabricating the deep trench capacitor may be carried out first, and then using the steps shown in Figs. 5C through 5E to form the active device. In this way, the problem due to having too large or too small a buried stripe window is similarly resolved.

[Para 54] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.